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### Circuit explanation of PLL initialization circuit

Because the output H of FF(H) is the L, through X8, FF(ABCD) and FF(E) are in ... it becomes the condition which X2, too, can pass the pulse signal through. ... Because it is, until the power supply becomes OFF when FF(H) turns over once ... It is to make count the 18 clocks at the 1 cycle including the LE signal ...

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two LC Low-pass filter of wide dynamic range and high-gain. The design of pulse generator unit is use of Altera ... And then it continues to count until the end of the ... appear the strongest signal pulse. Through trial and error ...

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